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## Enhanced Damage at Low Dose Rates in Linear Integrated Circuits

A. H. Johnston  
Jet Propulsion Laboratory  
California Institute of Technology  
Pasadena, California

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### Enhanced Damage

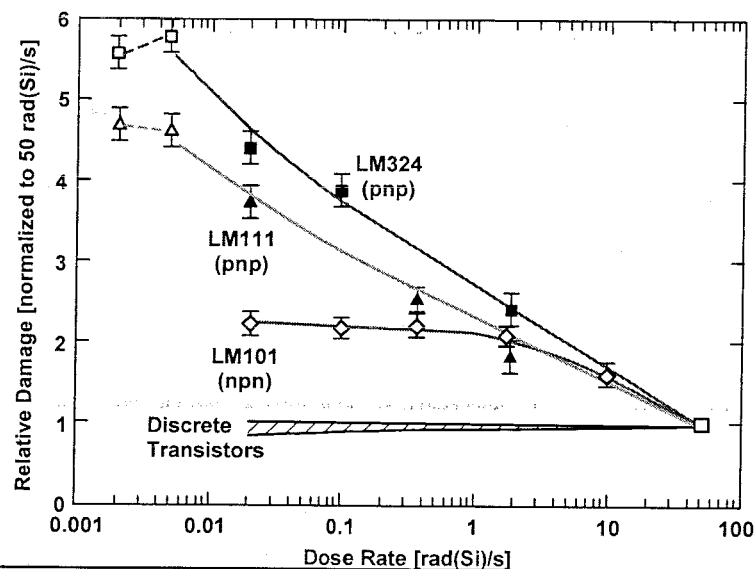
- First observed by Enlow, et al. in 1991
- Subsequent work by several laboratories has shown increased damage in many different circuits
  - Transistor damage can be 10 times more severe at low dose rate
  - Damage does not anneal (except at high temperature)

### Testing Issues

- Dose rates as low as 1 mrad(Si)/s may be required
- Damage may be more severe for unbiased devices
- Net effect in circuits can be quite complex
  - Several types of transistors are involved in circuit operation
  - Some critical parameters can change *abruptly*
  - Limits ability to apply safety factors in the absence of data at low dose rate
- Proton displacement damage must also be considered for linear circuits

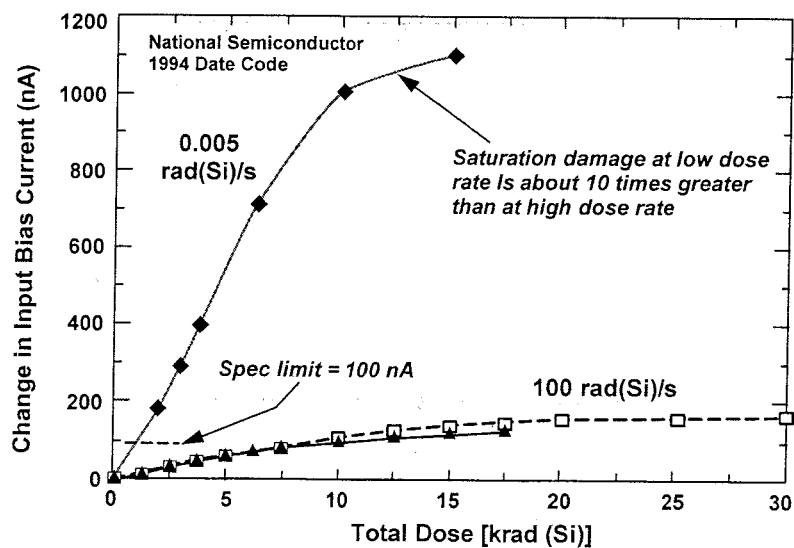
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**JPL** Low Dose Rate Effects on Various Transistor Types

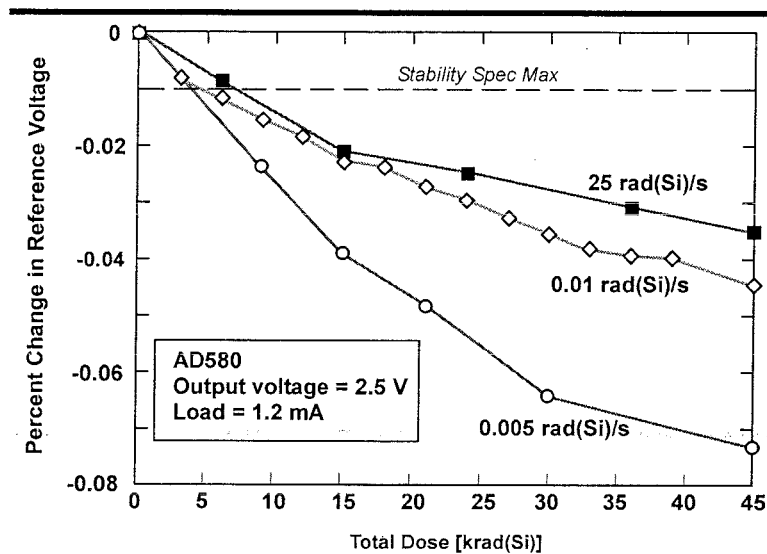


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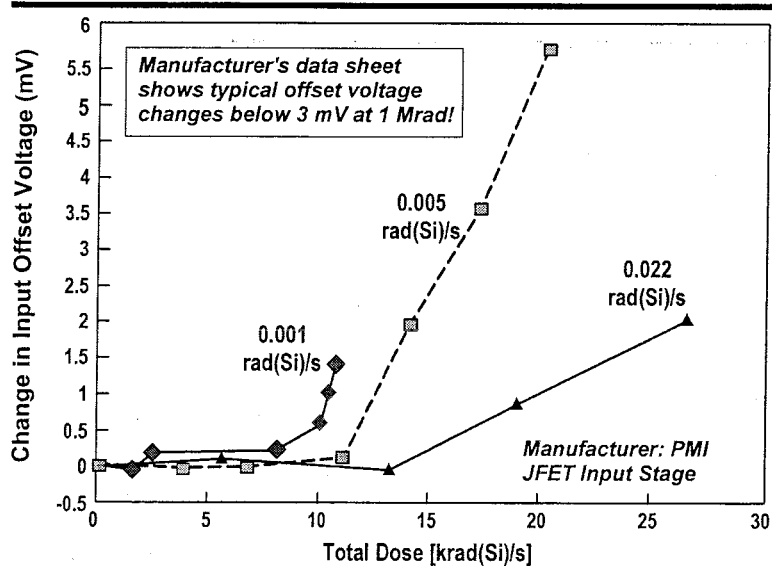
**JPL** Comparison of High and Low Dose Rate Damage



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National Semiconductor

Analog Devices

Only some devices

Devices with integrated JFET technology are particularly sensitive

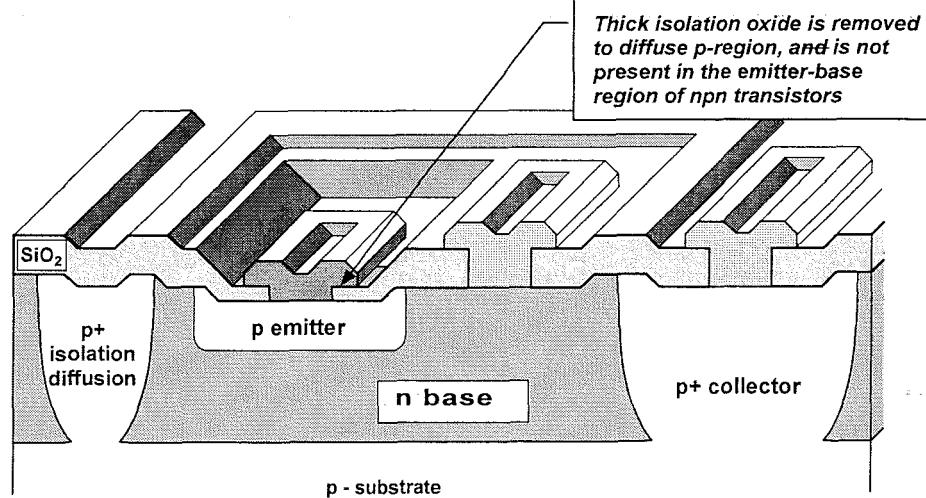
Linear Technology

Motorola

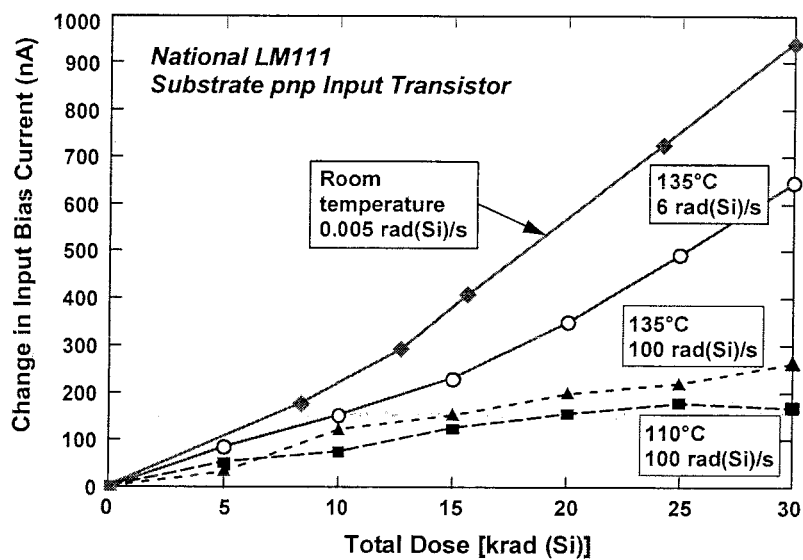
Micrel Semiconductor

Maxim Semiconductor (*BiCMOS process*)

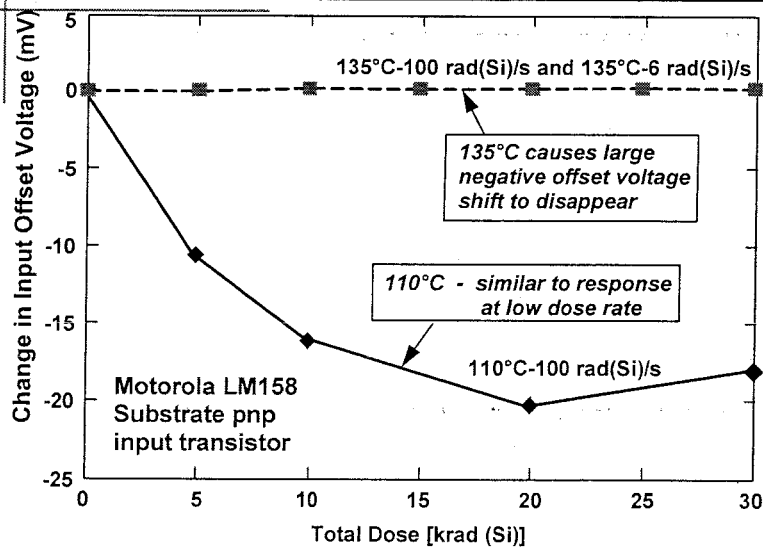
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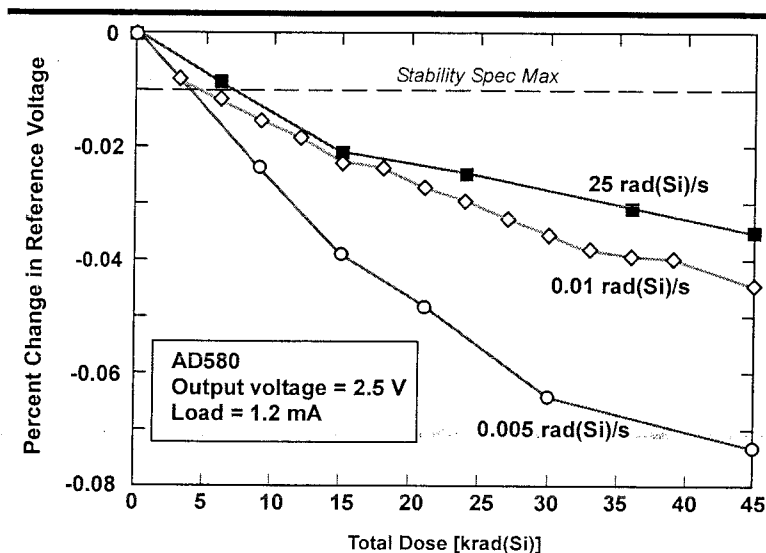
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## Work Questioning the Validity of High-Temperature Testing

JPL, Trans. Nucl. Sci., 1996

- Showed that damage annealed for some part types for  $T > 100^\circ\text{C}$
- Also showed that lower dose rate conditions were required at elevated temperature in order to simulate low dose rate effects

CNES (France), Trans. Nucl. Sci. 2000

- Examined wide range of devices
- Showed that tests at 0.55 rad/s and  $100^\circ\text{C}$  worked for input current, but not for offset voltage or other parameters
- Concluded that high-temperature acceleration was not a valid testing approach for many circuits

Univ. of Arizona/Aerospace (1996-1999)

- Demonstrated that different temperatures are required to accelerate damage in vertical, substrate and lateral transistors from the same process

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**Additional Tests under Various Circuit Conditions**

- Devices other than basic op-amps and comparators
- Wide range of use conditions

**Develop Recommended Test Approach for Linear Integrated Circuits**

- Existing Mil Standard (1019.5) is fatally flawed
  - Allows tests at elevated temperature in lieu of low dose rate under conditions that are blatantly incorrect
  - Result of forcing a simplified test method before the facts were in
- Two possible approaches
  - Require tests at low dose rate – reasonable option for most NASA missions
  - Allow tests at intermediate dose rate and elevated temperature
    - May require additional “safety factor”
    - Can’t guarantee that it will work for all devices

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**Devices Selected for Test**

- AD590 temperature transducer
- LM134 current source
- LT1185 low-dropout regulator
- LM139 (new National semiconductor process)

**Test Conditions**

- Biased and unbiased test at four dose rates
  - 2 mrad/s
  - 10 mrad/s
  - 200 mrad/s
  - 50,000 mrad/s
- High-Temperature Tests: 200 mrad/s @ 100 °C

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**Work to Date Shows that Radiation Tests at Low Dose Rate Are the Best Alternative**

- Total test time is about one month (20 krad, 5 mrad/s)
- High-temperature testing is clearly not valid for many devices
  - Requires extra work to verify that it is effective
  - Particularly difficult for low-dropout regulators and devices with low operating voltage

**JPL Test Matrix Is Nearing Completion**

- Determine viability of using high-temperature testing with additional safety factor
- Test standard will be completed by the end of FY02
  - Will include broader testing issues for linear circuits
  - Alternative approach will be given for missions with requirements above 30 krad where test times become too long

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**The Low Dose Rate Problem Is a Key Issue for NASA**

- Increasingly important for new linear designs with less operating headroom
- Lower amounts of shielding in small spacecraft will increase total dose levels

**Knowledge Base Has Focused too Strongly on LM111, LM124 and LM139**

- JPL test matrix will provide additional supporting data
- Mil Standard 1019.5 did not solve the problem
- New guideline is expected to be widely used within NASA

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